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10/773,333	02/09/2004	Hiroshi Okumura	Q77321	8920

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,333	OKUMURA, HIROSHI	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,14,16 and 29-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14,16 and 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/12/03 has been entered.

Response to Amendment

Amendment After Final Office Action filed 6/29/07 has been entered in light of aforementioned Request for Continued Examination. In said Amendment Applicant substantially amended the Specification. Comments on Remarks field with said Amendment are included below under "Response to Arguments".

Specification

The Amendment to the Specification has been approved.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 29, 16, 33 and 34*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view Osamu Nakamura (JP 2003-017502A) (made of record by Applicant in IDS filed 6/9/05 and previously cited), or, in an alternative rejection: over said Prior Art as Admitted by Applicant in view of both Osamu Nakamura (JP 2003-017502A) (previously cited) and Kenichi Nakamura (6,133,609), henceforth referred to as "Nakamura2".

Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a low voltage driving thin film transistor (driver transistor with gate 304 *capable* of being driven by low voltage) formed above said insulating substrate (cf. Figure 1), comprising a first active layer 302 (island-like portion to the left in Figure 1 comprising 305a; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a high voltage driving thin film transistor (pixel transistor with gate 307 *capable* of being driven by high voltage) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1 comprising 305b; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on

said second active layer, a second gate electrode formed 307 (see [03]) and capable of being driven at high voltage being formed on said second gate insulating film,

wherein said second gate insulating film 303/306 comprises said first gate insulating film 303 (Figure 1) and a gate cover 306 (Figure 1 and [0005]) formed above said first gate insulating film (lco.cit and Figure 1),

wherein said second active layer has at least two impurity doping regions 305b on both sides of the channel ([0005]).

Prior Art as admitted by Applicant does not necessarily teach the further limitations

(a) said "at least two impurity doping regions" are "formed in a self-aligning manner with respect to said first gate electrode";

(b) "wherein said high voltage driving thin film transistor further comprises a third gate electrode driven at low voltage and formed between said second active layer and said second gate electrode with gate length shorter than that of the second gate electrode";

(c) the limitations "low voltage driving" (lines 3-4), "high voltage driving" (lines 7-8 and 19), "driven at low voltage" (lines 6 and 20), "driven at high voltage" (line 10), and generically any limitation on whether or not any thin film transistor is driven at a high or at a low voltage is a limitation on intended use rather than the thin film transistor itself: intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See MPEP 2111-2114.

With regard to limitation (a), *the limitation "formed in a self-aligning manner with respect to said gate electrode"* only has patentable weight in the result for the final structure and constitutes a product-by-process limitation and is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See MPEP 2113, from which it is clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

In the underlying case, forming impurity doping regions in a self-aligning manner is known to strongly reduce the overlap between gate and source/drain regions. However, the claim does not quantify this reduction, neither does the specification quantify the difference between gate source/drain overlap with and without self-alignment using the gate as mask, because said overlap can be 0.1 microns when self-alignment is used and is allowed to vary between 0 and 2.0 microns if self-alignment is not used, as witnessed by claims 13 and 30. Therefore, no definite property of the final structure is implied by the step of forming the impurity doping regions (see rejection above under 35 USC 112, second paragraph). Because no definite final structure ramification can be discerned no patentable weight is given to the limitation "formed in a self aligning manner".

Furthermore, it would have been obvious to include the further limitation ad (b) in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode 13 between an active layer and a gate electrode 17 with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

Furthermore, gate electrode 17 by Nakamura et al has a length that exceeds the length of gate electrode 13 (see front Drawing) and hence the range limitation on gate lengths is met in the Prior Art as cited. A *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as claimed do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties.

In addition to the aforementioned rejection, in the following alternative rejection, it would have been obvious to operate said third electrode at a voltage lower than said second electrode in view of Nakamura2 because of his teaching to operate high-voltage transistors 101 and 102 (col. 3, l. 19-27) with main-gate electrodes 4 and 12 (col. 3, l. 35-56) self-aligned with the first and second active regions 71 and 72 (col. 3, l. 35-56) on a first gate insulating film 3 (col. 3, l. 36) and sub-gate electrodes 11 and 15 (col. 3, l. 38-41 and col. 3, l. 53-56) above said main-gate electrodes, said sub-gate electrodes operable, and in fact: operated, at a different, specifically: higher voltage than the main-gate electrodes (col. 6, l. 5-10) so as to control the resistance of a region between the

heavily doped source/drain regions (col. 3, l. 66 – col. 4, l. 4 and col. 4, l. 15-20) and overlapping with said sub-gate electrodes (51/61 and 52/62 for the respective transistors 101 and 102) (see col. 3, l. 66 – col. 4, l. 4 and col. 4, l. 15-20); from which follows that in a high-voltage transistor it would have been obvious to structure the device to allow for independent setting of voltages for the equivalents of electrodes 13 and 11 of Nakamura as cited previously and in particular to allow in Nakamura (JP 2003-017502) as previously cited for a *higher* voltage of electrode 11 in operation than for electrode 13, so as to have independent control of the resistivity of the underlying peripheral region of the channel. *Motivation* immediately derives from said independent control.

On claim 16: at least one of said impurity doping regions that overlap said second gate electrode includes an LDD structure 14 (see English abstract in Nakamura), which would have been obvious to include in the prior art as admitted by Applicant because LDD regions counteract hot electron effects. *Motivation* to include the teaching on LDD structure by *Nakamura* is the avoidance of hot electron effects in the high-voltage transistor.

On claim 34: said first gate electrode 304, said second gate electrode 307 in the prior art as admitted by applicant are formed under wires which connect to said impurity doping regions 305a and 305b, respectively. Inclusion of the third gate electrode (as shown would have been obvious over Nakamura) necessarily places said gate electrode between the active layer and the second gate electrode according to claim 29

and hence places said third gate electrode also under said wires that connect to said impurity doping regions.

2. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant and Nakamura, and, in the alternative, over Prior Art by Applicant, Nakamura and Nakamura2 as applied to claim 29 above, and further in view of Adler et al (5,757,050) (previously cited). As detailed above, claim 29 is unpatentable over Prior Art as admitted by Applicant, in view of either Nakamura or Nakamura and Nakamura2, none necessarily teaching the further limitation defined by claim 13. However, it would have been obvious to include said further limitation in view of Adler et al who teach a thin film transistor that is self-aligned (col. 2, l. 50-59) and with overlap by 0.1 mm or less (col. 8, l. 24-43). Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as claimed do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

3. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant and either Nakamura or Nakamura and Nakamura2 as applied to claim 29 above, and further in view of Zhang et al (6,507,069 B1) (previously cited). As detailed above, claim 29 is unpatentable over Prior Art as admitted by Applicant in view of Nakamura or Nakamura and Nakamura2, none however necessarily teaching the further limitation defined by claim 14. However, it would have been obvious to

include said further limitation in view of Zhang et al, who, in a patent on thin film transistors, hence analogous art, teach self-aligned thin film transistors to include LDD regions for the specific reason to reduce the OFF current (col. 2, l. 9-15). *Motivation* to include the teaching by Zhang thus derives from the obvious advantage to reduce the inherently unwanted current in the OFF state.

4. ***Claim 30*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant and either Nakamura or Nakamura and Nakamura2 as applied to claim 29, and further in view of Izawa et al (5,053,849) (previously cited).
As detailed above, claim 29 is unpatentable in view of Prior Art as Admitted by Applicant, in view of Nakamura or Nakamura and Nakamura2. Neither reference necessarily teaches the further limitation defined by claim 30. *However, it would have been obvious to include the further limitation in view of Izawa et al*, who, in a patent on overlapping gate/drain gate structures (see title), hence analogous art, teach the overlap to be about 0.2 mm (col. 13, l. 53-66), which overlaps the range as claimed. A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

5. ***Claims 31-32*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant and either Nakamura or Nakamura and Nakamura2

as applied to claim 29, in further view of Numasawa et al (6,048,795) (previously cited). As detailed above, claim 29 is unpatentable over Prior Art as Admitted by Applicant in view of either Nakamura or Nakamura and Nakamura2. Neither reference necessarily teaches the further limitation defined by claim 31. *However, it would have been obvious to include the further limitation ad (c) in view of Numasawa et al*, who, in a patent on gate electrodes formed in a self-alignment process step with source and drain regions (see Figure 2E and col. 1, l. 17-52), hence analogous art, teach the gate electrode to comprise a two –layer structure including a semiconductor layer 13 (hence claim 32 is also met) and a metal layer 14 (col. 3, l. 25 – col. 4, l. 58). *Motivation* to include the teaching by Numasawa et al in the invention of the Prior Art derives from the advantage of increased electric conductivity of the gate electrode without having to give up the convenience of the self-alignment process step in creating source and drain regions with the gate as mask (col. 1, l. 16-30).

6. ***Claim 33*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant and either Nakamura or Nakamura and Nakamura2 as applied to claim 29 above, and further in view of Suzawa et al (5,914,498) (previously cited).

As detailed above, claim 29 is unpatentable over Prior Art as Admitted by Applicant, in view of Nakamura or Nakamura and Nakamura2. Neither said Prior Art as Admitted by Applicant nor Nakamura nor Nakamura2 necessarily teach:

(A) the further limitation that said third gate electrode is formed of the same material as said first gate electrode; nor the further limitation;

(B) that said third gate electrode has the same thickness as said first gate electrode. *However, it would have been obvious to include the limitations (A) and (B) in view of Suzawa et al*, who teach gate electrodes displaced substantially laterally from each other to be made of the same material (aluminum 105/106: Figure 1A and col. 5, l. 20-27) and to have the same thickness (as witnessed by the reference to the thickness of the gate electrodes: see col. 14, l. 68 and col. 15, l. 1). Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416; and, furthermore, that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Response to Arguments

Applicant's arguments filed in Remarks submitted with said Amendment have been fully considered but they are not persuasive. Specifically, although the amendment to the Specification has been approved, counter to applicant's allegation (page 4) that "[T]he electrode 17 taught by Nakamura cannot possibly correspond to a gate electrode because the electrode 17 does not overlap the channel region" is incorrect on more than one point:

(1) Gate electrodes often overlap LDD regions, as witnessed for instance by Wolf, page 592.

(2) The electrode 17 does produce an electric field of importance at least in the LDD regions, which is a trivial consequence from its connection to said gate electrode 13: see paragraph [0039] of Nakamura stating that an electric field "is given" "to the LDD regions by electrode 17, although weaker than the electric field which gate electrode 13 gives to the semiconductor layer". Parenthetically, it is noted that whether the electric field in the LDD regions caused by electrode 17 is weaker or stronger than the electric field in the semiconductor layer caused by electrode 13 is a matter of a disclosed method of use rather than a structurally inherent property of the device by Nakamura and furthermore not only depends on the voltages on the electrodes, but also on the relation between the different distances to said electrodes at which the aforementioned electric fields are produced.

(3) The electric field produced by electrode 17 in the non-doped portion of the channel only differs from the electric field produced in the LDD regions by a geometric factor of the order of unity, as simple geometry shows, particularly since the LDD region and the central un-doped portion of the channel abut.

Therefore, applicant's insistence on words (page 5, second paragraph) fails to have technical basis.

Furthermore, applicant's criticism of the rejection allegedly because of an oversight of the amendment of claim 29 (from central paragraph of page 5 up to and including page 6 of Remarks) is incorrect: Nakamura et al is cited for gate electrode 13

in the multi-gate electrode transistor, while applicant's argument once again hinges on the lack of operability of electrode 17 as gate electrode, which has been answered in the foregoing discussion, which discussion is herewith included by reference. Once again: paragraph [0039], produces is a gate electrode because a gate potential and because it influences the electric field in the channel region, again with reference to [0039] in Nakamura.

Finally, applicant's allegation on separate high and low voltages for electrodes corresponding to electrodes 13 and 17 is not entirely persuasive either because the imposition of specific values of voltage to one with respect to the voltage of another gate electrode can be considered a matter of intended use. The nature of the electrical connection between the second and third electrode as taught by Nakamura is not specified and hence the relation between the voltages of the two electrodes does not necessarily follow as the only possible one from the device as disclosed.

However, for efficiency of prosecution Nakamura (6,133,609) has been cited in the present rejections, because of his teaching to operate high-voltage transistors 101 and 102 (col. 3, l. 19-27) with main-gate electrodes 4 and 12 (col. 3, l. 35-56) self-aligned with the first and second active regions 71 and 72 (col. 3, l. 35-56) on a first gate insulating film 3 (col. 3, l. 36) and sub-gate electrodes 11 and 15 (col. 3, l. 38-41 and col. 3, l. 53-56) above said main-gate electrodes, said sub-gate electrodes operable, and in fact: operated, at a different, specifically: higher voltage than the main-gate electrodes (col. 6, l. 5-10) so as to control the resistance of a region between the heavily doped source/drain regions (col. 3, l. 66 – col. 4, l. 4 and col. 4, l. 15-20) and

overlapping with said sub-gate electrodes (51/61 and 52/62 for the respective transistors 101 and 102) (see col. 3, l. 66 – col. 4, l. 4 and col. 4, l. 15-20); from which follows that in a high-voltage transistor it would have been obvious to structure the device to allow for independent setting of voltages for the equivalents of electrodes 13 and 11 of Nakamura as cited previously and in particular to allow in Nakamura (JP 2003-017502) as previously cited for a *higher* voltage of electrode 11 in operation than for electrode 13, so as to have independent control of the resistivity of the underlying peripheral region of the channel.

In conclusion, in light of continued examination the claims as amended are unpatentable over Prior Art as Admitted by Applicant in view of either Nakamura (JP-2003-017502), or, in the alternative, in view of Nakamura (JP 2003-017502) in view of Nakamura (6,133,609), in the rejections referred to as "Nakamura2", with reference to the rejections provided overleaf, which are herewith included in this "Response to Arguments" by reference in their entirety.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM

September 15, 2007

Primary Patent Examiner:

Johannes Mondt (TC3600, Art Unit: 3663).